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10/24/00

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for nonprovisional applications under 37 CFR § 1.53(b))

Attorney Docket No	500080.02
First Inventor or Application Identifier	Thomas W. Voshell
Title	METHOD AND APPARATUS FOR REDUNDANT LOCATION ADDRESSING USING DATA COMPRESSION
Express Mail Label No.	EL673947162US

JC926 U.S. PTO 09/695756 10/24/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Box Patent Application
Commissioner of Patents
Washington, D.C. 20231

1. [X] General Authorization Form & Fee Transmittal (Submit an original and a duplicate for fee processing)
2. [X] Specification [Total Pages] 21
   (preferred arrangement set forth below)
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) [Total Sheets] 5
4. Oath or Declaration [Total Pages] 1
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 17 completed)
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [X] Incorporation By Reference (useable if box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program (Appendix)
7. Nucleotide and Amino Acid Sequence Submission (if applicable, all necessary)
   a. [ ] Computer-Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [X] 37 CFR 3.73(b) Statement (when there is an assignee) [X] Power of Attorney
10. [ ] English Translation Document (if applicable)
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. [X] Other: Certificate of Express Mail
    Copy of Revocation and Substitute POA
    Check

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information below and in a preliminary amendment*

[x] Continuation [ ] Divisional [ ] Continuation-In-Part (CIP) of prior Application No.: 09/012,036 Filed January 22, 1998

Prior application information: Examiner Samuel Lin Group / Art Unit 2784

[ ] Claims the benefit of Provisional Application No. ____

CORRESPONDENCE ADDRESS

Kimton N. Eng, Esq.
Dorsey & Whitney LLP
1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101-4010
(206) 903-8800 *phone*
(206) 903-8820 *fax*

Respectfully submitted,

TYPED or PRINTED NAME Kimton N. Eng REGISTRATION NO. 43,605

SIGNATURE Kimton Eng Date October 24, 2000

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EXPRESS MAIL NO.: EL673947162US

PATENT

JC926 U.S. PTO
09/695756
10/24/00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Thomas W. Voshell Attorney Docket No.: 500080.02

Filed : Concurrently herewith

Title : METHOD AND APPARATUS FOR REDUNDANT LOCATION ADDRESSING USING DATA COMPRESSION

GENERAL AUTHORIZATION UNDER 37 C.F.R. § 1.136(a)(3) AND FEE TRANSMITTAL

Box Patent Application
Commissioner of Patents
Washington, D.C. 20231

Sir:

With respect to the above-identified application, the Commissioner is authorized to treat any concurrent or future reply requiring a petition for an extension of time under 37 C.F.R. § 1.136(a)(3) for its timely submission as incorporating a petition therefor for the appropriate length of time. The Commissioner is also authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account No. 50-1266.

With respect to the above-identified application, the fee is calculated below:

For	Number Filed	Number extra		Rate		
Basic Fee						$ 710
Total Claims	1	0	X	$ 18	=	$ 0
Independent Claims	1	0	X	$ 80	=	$ 0
TOTAL FILING FEE						**$ 710**

A check in the amount of $710 is enclosed to cover the filing fee.

The Commissioner is authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 which may be required, or credit any overpayment, to Deposit Account No. 50-1266. A duplicate copy of this request is enclosed.

Date October 24, 2000

Kimton N. Eng

Kimton N. Eng
Registration No. 43,605

KNE:ca

Enclosure:
Copy of this General Authorization

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800
Fax (206) 903-8820

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

JC926 U.S. PTO 09/695756 10/24/00

Applicant : Thomas W. Voshell Attorney Docket No.: 500080.02

Filed : October 24, 2000

Title : METHOD AND APPARATUS FOR REDUNDANT LOCATION ADDRESSING USING DATA COMPRESSION

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Box Patent Application
Commissioner of Patents
Washington, D.C. 20231

Sir:

I hereby certify that the enclosures listed below are being deposited with the United States Postal Service "EXPRESS MAIL Post Office to Addressee" service under 37 C.F.R. § 1.10, Mailing Label Certificate No. EL673947162US, on October 24, 2000, addressed to Box Patent Application, Commissioner of Patents, Washington, DC 20231.

Respectfully submitted,

DORSEY & WHITNEY LLP

Jeanette West

/ for West Courier

KNE:ca

Enclosures:

- Postcard
- Check
- Form PTO/SB/05
- General Authorization Under 37 C.F.R. § 1.136(a)(3) and Fee Transmittal (+ copy)
- Preliminary Amendment
- Specification, Claims, Abstract (21 pages)
- 5 Sheets of Drawings (Figures 1-5)
- Copy of Declaration
- Copy of Election and Power of Attorney
- Copy of Revocation and Substitute Power of Attorney
- Information Disclosure Statement and Form PTO-1449

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EXPRESS MAIL NO.: EL673947162US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Present Application:

Applicant	:	Thomas W. Voshell
Attorney Docket No.	:	500080.02
Filed	:	Concurrently herewith
Title	:	METHOD AND APPARATUS FOR REDUNDANT LOCATION ADDRESSING USING DATA COMPRESSION

Prior Application:

Examiner	:	Samuel Lin
Art Unit	:	2784
Serial No.	:	09/012,036

PRELIMINARY AMENDMENT

Box Patent Application
Commissioner of Patents
Washington, D.C. 20231

Sir:

Please amend the above-identified application as follows:

In the Specification:

Amend the specification by inserting a new section before the "Technical Field" as follows:

-- CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of pending United States Patent Application No. 09/012,036 , filed January 22, 1998. --

In the Claims:

Please cancel claims 2-40, leaving claim 1.

Respectfully submitted,

DORSEY & WHITNEY LLP

Kimton N. Eng

Kimton N. Eng
Registration No. 43,605

KNE:ca

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

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METHOD AND APPARATUS FOR REDUNDANT LOCATION ADDRESSING USING DATA COMPRESSION

TECHNICAL FIELD

This invention generally concerns memory arrays, and more particularly, techniques for identifying and substituting for defective locations in memory arrays.

BACKGROUND OF THE INVENTION

Memory arrays consist of a number of storage locations or memory cells. Memory arrays are generally coupled to a storage control unit for accessing storage locations (cells) in order to store information in, or to retrieve information from, the memory array. Memory arrays are generally constructed in a reliable and robust manner. However, some random number of memory locations may be or become defective. It is desirable to avoid storing data to, or retrieving data from, defective memory locations. In order to avoid accessing defective memory locations, a memory map is generally devised to map addresses for defective memory array cells to another memory array or another portion of the memory array that is known to be operative. This memory array or portion is commonly referred to as a spare or a redundant memory array. The memory map is stored in another memory array, known as the map memory array. The size required for the spare and map memory arrays depends on the number of defective memory cells to be replaced. If the primary or first memory array requires that all locations be spared, the spare memory array will need to be as large as the first memory array and the map memory array will also need to be large. Since relatively few locations in the first memory array usually are defective, the size of the spare memory array is usually far less than the size of the primary or first memory array. It is desirable, of course, to make the spare and map memory arrays as small as possible, as unused locations dedicated to spare or map memory are wasted and this wastes resources. In order to

maximize the efficient use of memory resources, there is need for a method and corresponding apparatus for reducing the amount of data to be stored in the map memory array.

SUMMARY OF THE INVENTION

Briefly stated, in a first embodiment, the present invention contemplates a method for identifying defective cells in a memory array. The method includes steps of receiving a request for accessing an address and analyzing the address to determine when the address matches an address stored in a temporary memory array. When the address does not match any address stored in the temporary memory array, the method includes steps of sending a wait instruction, analyzing the address to determine which portion of compressed data stored in a map memory array to decompress and decompressing the portion of compressed data to provide expanded data. The method also includes steps of writing the expanded data to the temporary memory array and comparing the expanded data to the address to determine when the address corresponds to an expanded datum of the expanded data.

In a second embodiment, the present invention includes a method for accessing a memory array. The method includes steps of requesting an address for one or more memory array cells comprising a first memory array and comparing the address to decompressed data describing defective memory array cells in the first memory array to determine when the address and a datum from the decompressed data match. The method includes a step of routing the address to a second memory array when the address and a datum from the decompressed data match.

In a third embodiment, the present invention includes a method for accessing a memory array. The method includes steps of receiving a memory array access request including a requested address, generating a first hash code from the requested address and comparing the first hash code to hash codes for decompressed addresses stored in a temporary memory array. When a match is

found between a hash code for a decompressed address and the first hash code, the method includes a step of routing the memory array address request to a spare memory array.

Another embodiment of the present invention includes a memory control circuit. The memory control circuit includes a storage control unit coupled to a bus. The storage control unit accesses memory array units to retrieve data from a first memory array unit in response to memory array access requests delivered via the bus. The memory control circuit also includes a first memory array coupled to the storage control unit. The first memory array is for temporarily storing data. The memory control circuit additionally includes a second memory array coupled to the storage control unit. The second memory array provides cells for replacing cells determined to be defective in the first memory array. The memory control circuit further includes a data compression circuit that compresses data describing memory array addresses corresponding to cells determined to be defective in the first memory array to provide compressed addresses. The data compression circuit also decompresses compressed addresses to provide decompressed addresses. The data compression circuit couples to the storage control unit.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a computer system employing a compression engine in accordance with an embodiment of the present invention.

Figure 2 is a block diagram of the memory storage control unit in a preferred embodiment of the invention.

Figure 3 is a flowchart of a process for testing a memory array in accordance with another embodiment of the invention.

Figure 4 is a flowchart of a process for accessing primary and spare memory array cells in accordance with yet another embodiment the invention.

Figure 5 is a flowchart of a portion of the process of Figure 4, where the portion determines when a given memory cell location is defective.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 is a block diagram of a computer system 10 that uses one embodiment of the present invention. The computer system 10 includes a central processing unit or CPU 12 coupled by a bus 17 to an input/output or I/O device 15 and to a storage control unit 20. In a preferred embodiment, the CPU 12 may be a 68040 processor available from Motorola of Phoenix, Arizona or a Pentium ® processor available from Intel of Santa Clara, California. I/O device 15 may comprise a keyboard, one or more disk data storage units, a display, a printer or coupling to external data sources such as a local area network or the like.

The storage control unit 20 couples via the bus 17 to a collection of memory devices including ROM 31, RAM 35 (*i.e.*, the primary memory or first memory array), a spare memory array 39, a map memory array 41 and a temporary memory array 43. The spare memory array 39, map memory array 41 and/or temporary memory array 43 may be included within the storage control unit 20, may comprise sections of RAM 35 reserved for this purpose or may comprise separate memory units.

The storage control unit 20 is coupled via bus 17 to the map memory array 41 and the temporary memory array 43. In operation, the CPU 12 operates on data from the I/O device 15 in response to commands retrieved from memory, either from ROM 31 or RAM 35 via the storage control unit 20, and also stores data via the storage control unit 20 into RAM 35. Memory cells in each of the memories ROM 31, RAM 35, spare memory array 39, map memory array 41 and temporary memory array 43 include a regular arrangement having a fixed number of dimensions. These dimensions are ordered in some fashion, *e.g.*, page, row and column. Each of these dimensions are then subdivided and numbered, for example, page 1, 2, 3 and the like. This common scheme specifies a regular structure, repeating for some interval. This also allows for easy accessing of data stored in the memory array as the page number, row number and column number are all that is necessary to access memory cells for

information storage or retrieval. Because of the regular structure of the memory array, creating a map to direct retrieval or storage to spare memory cell locations in the spare memory array 39 for replacement of defective memory cells in, *e.g.*, RAM 35, is also simplified.

For example, if page 3, row 16, column 32 is the location of a defective storage cell, the map may need only the numbers 3, 16, 32 in order to provide a replacement memory cell. Replacement locations are normally assigned on a first come, first served basis. Thus, for every entry in the map memory array 41, a sequential replacement location may be assigned in the spare memory array 39. While this method allows efficient and easy access to replacement memory cells in the spare memory array 39, certain types of defects consume large amounts of the map memory array 41 storage space.

In the case where errors are not in a random distribution, *e.g.*, burst errors where multiple cells are centered around a particular location, or the loss of an entire dimension in the memory array, such as the loss of an entire row or column, significant efficiencies may be gained in utilization of the map memory array 41 using data compression to reduce the map data size required to store the addresses of the defective memory cells in the map memory array 41 prior to storage. For example, if page 0, row 10, column 13 in RAM memory array 35 had 192 consecutive defective locations on it, starting with the first location, then a simple data compression saving 191 map locations is effected by representing the defects in the RAM memory array 35 with the record 0, 10, 13, 192. This is a relatively primitive approach to data compression, however, it illustrates the basic principle. When more sophisticated compression algorithms are used, greater compression efficiency may be achieved.

In the operation of the computer system 10 of Figure 1, the storage control unit 20 scrutinizes all memory access requests. When a particular memory access request matches an address encoded in the compressed data stored in the map memory array 41, *e.g.*, as discussed with respect to Figures 3 through 5, an address in the spare memory array 39 is substituted for the

requested address. This substituted address selects a memory cell from the spare memory array 39 instead of, for example, from RAM 35. This process requires some portion of the data in the map memory array 41 to be decoded from the compressed state (as stored in the map memory array 41), in order to utilize defective cell address data from the map memory array 41.

One way of accomplishing this is to use a hash coding algorithm. During data compression within storage control unit 20, a code word may be generated that points to each defective cell address from the RAM 35 mapped in the map memory array 41. A cyclic code or some other robust process may be used to quickly produce a unique code word for each defective cell address in the primary memory. This code word represents a "hash code" and may be used as an index into the decompressed addresses and their associated hash codes stored in temporary memory array 43.

One way to generate hash codes is to treat the address data as a contiguous series of bits, *i.e.*, as a number. This number is then divided by a prime number, such as 11. The most significant bits of the hash code provide an estimate of the address data and is useful as a quick index to a given number of replacement records in the map memory array 41.

When a hash code matching one of the hash codes stored in the temporary memory array 43 is produced by analysis of the address for the accessed memory cell site, the matching record in the temporary memory array 43 is used to redirect access to the spare memory array 39. When the comparison of the hash code for the address to which access is sought to the hash codes stored in the temporary memory array 43 produces a "miss" *i.e.*, the defective cell addresses in the primary memory array 35 are not available in expanded form in the temporary memory array 43, a wait request may be issued to the CPU 12 while the data stored in the map memory array 41 are decompressed by the storage control unit 20.

Alternatively, an estimate may be made as to the range of memory array addresses required and some of the compressed data from the map memory

array 41 may be uncompressed by the storage control unit 20 and then stored in the temporary memory array 43. A least-recently-used algorithm may be used to specify replacement cell addresses from the temporary memory array 43.

In a preferred embodiment, the storage control unit 20 of Figure 1 is realized as illustrated by the block diagram of Figure 2. A first component 201 acts as a compression engine, to provide compressed data to, and to decompress compressed data from, the map memory array 41. The first component 201 also acts to set a compression flag for the hash code in the hash code storage area of the map memory array 41. A hash code generator 203 generates hash codes from addresses using any known method for providing truncated codes as indices. A hash code correlator 205 takes error location and hash code data and uses the hash code to quickly approximate addresses corresponding to bad cell address data stored in the map memory array 41. A relocation record register 207 stores one relocation record to provide access to relocated data, *i.e.*, data corresponding to the address currently being accessed in spare memory array 39.

A hash code register stack 209 stores hash codes for uncompressed address data from the map memory array 41 that are stored in the temporary memory array 43. The hash code register stack 209 provides quick reference to the storage addresses corresponding to defective memory locations in RAM 35 that have been most recently accessed and includes records for hash codes corresponding to memory locations that are currently stored in an uncompressed state, for example, in temporary memory array 43. An error detection code generator 211 provides and stores a check code every time a memory location is accessed for a write operation. When the same memory location is read, another check code is generated and is compared with the earlier check code generated during the write operation. When the two code words differ, an error has occurred. The error check operation may be implemented using any known method, including methods as simple as parity checking or as thorough as the Reed-Solomon technique.

The storage control unit 20 then analyzes the address to determine if it is the address of a location known to have failed, using a hash code that is calculated when a memory cell test indicates a defective memory cell. When there is a match between the hash code for the current address to which access is sought and a stored hash code in the storage control unit 20, the storage control unit 20 fetches the relocation record from the relocation record register 207 using the using the address as a key, obtains the address in the spare memory array assigned to the requested address and substitutes this spare memory array address for the requested address. When there is no match between the hash code for the current address to which access is sought and a stored hash code in the storage control unit, the current address is treated as an address for a defective memory cell as described with reference to the initial memory testing (see Figures 3-5 and associated text). In either case, an address translator 213 passes the correct address in the spare memory array 39 to the bus 17. A least-recently-used/most-recently used register 215 maintains counts to accesses to hashed locations, *i.e.*, to accesses to addresses within the spare memory array 39.

While Figure 2 shows the computer system 10 as implementing the storage control unit 20 as a stand-alone unit, it will be appreciated that storage control unit 20 or one or more of the associated functions may be implemented in a number of other ways. For example, one or more of the functions of the storage control unit 20 may be included in software or in instructions contained in the ROM 31 and executed by the processor 12. Alternatively, one or more of the functions of the storage control unit 20, the spare memory array 39, the map memory 41 and the temporary memory array 43 may be implemented in the integrated circuit(s) comprising RAM 35.

Figure 3 is a flow chart of a process 50 for testing a memory array to generate addresses of defective memory array cells in, for example, RAM 35, for compressing data describing defective memory array cell locations and for storing the compressed data describing defective memory array cell locations in the map memory array 41. Generally, the process 50 may be invoked on any sort

of power on, reset or boot operation in step 52, or in response to other criteria such as a memory test command. Memory array cell testing begins in step 54 and then a query task 56 is invoked to determine if a given cell is defective. When the given cell is not defective, control passes to a query task 60 to determine whether or not that cell is the last cell to be tested. When the cell tested in the query task 56 is defective, the cell address is written to a temporary memory that is known to operate properly in step 58. Control then passes to the query task 60 again. When this is not the last cell to be tested, the process 50 advances to the next cell in step 62 and reinitiates the query task 56.

When the query task 60 determines that the last cell in the array has been tested, defective memory array cell address data are compressed in step 64, for example, via the storage control unit 20 of Figure 1. The compressed data are stored in the map memory array 41 in step 66. The process 50 then ends in step 68.

The process 50 thus tests, for example, all memory locations in RAM 35 during a power on or reset operation, or any other type of reset operation (or in response to a memory test command). The process 50 gleans information describing defective memory array cell address data for RAM 35, compresses those data and then stores the compressed data in the map memory array 41.

Figure 4 is a flow chart of a process 70 for processing memory array address requests. The process 70 begins in step 72 with a request to access one or more memory array cells in step 74. In a query task 76, the storage control unit 20 determines if the address to which access has been requested is for a defective memory array cell. This is discussed in more detail below with reference to Figure 5. When the query task 76 determines that the address does not correspond to a defective memory array cell in, for example, RAM 35, RAM 35 is accessed in step 78. Control then passes to a query task 84 to determine whether or not all memory array access requests have been executed. When all memory array access requests have been executed, the process 70 ends in step

86. When not all memory array access requests have been processed, control passes to request access to one or more memory array cells in step 74.

When the query task 76 determines that a requested address is for a defective memory array cell, a spare memory array address is obtained from the temporary memory array 43 in step 80, and a cell in the spare memory array 39 is accessed in step 82. Control then passes to the query task 84 to determine whether or not all memory array access requests have been executed.

Figure 5 is a flow chart showing the query task 76 in more detail. The query task 76 begins with a query task 90 to determine if the address is in a range of addresses stored in the temporary memory array 43. When the requested address is in the range of addresses stored in the temporary memory array 43, control passes to a query task 100 to determine if the requested address corresponds to a defective memory array cell. The "yes" and "no" options of the query task 100 correspond to the "yes" and "no" options shown with query task 76 of Figure 4.

When the address that is requested is not in the range of the temporary addresses stored in the temporary memory array 43, an optional "wait" signal may be passed in step 92 to the unit requesting memory access, such as the CPU 12 of Figure 1. In one embodiment, a range of data to be decompressed from the map memory array 41 are estimated in step 94, and data falling within this range are decompressed in step 96 via the storage control unit 20 of Figure 1. The decompressed address data are stored in step 97 in the temporary memory array 43 of Figure 1. An optional "end wait" signal may then be sent in step 98 to the unit requesting memory access, for example, the CPU 12. Control then passes back to the query task 100 to determine if the requested address corresponds to one of the decompressed addresses for defective memory cells stored in the temporary memory array 43.

The invention as described may allow a memory array to be operated more efficiently by reducing the number of memory cells needed in order to store a map of defective memory cells in the memory array. It may be

integrated into a memory chip, implemented in software or by discrete components or it may be employed together with memory devices in a larger system.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

1. A method for identifying defective cells in a memory array, the method comprising steps of:

receiving a memory test command;

initiating a memory test in response to the memory test command, the memory test for determining addresses of defective cells in a random-access memory;

concluding the memory test; and

compressing the addresses of defective cells to provide compressed address data.

2. A method as claimed in claim 1 wherein the step of initiating a memory test includes a step of storing addresses of defective cells in a temporary memory array.

3. A method as claimed in claim 1, further including a step of storing the compressed address data in a map memory array.

4. A method for accessing a memory array, the method comprising steps of:

requesting an address for one or more cells comprising a first memory array;

analyzing the address to determine when the address matches an uncompressed address in a temporary memory array, and, when the address does not match any uncompressed address stored in the temporary memory array, the method includes steps of:

analyzing the address to determine which portion of compressed data stored in a third memory array containing compressed addresses of defective cells in the first memory array to decompress;

decompressing the portion of compressed data to provide expanded data;

writing the expanded data to the temporary memory array;

comparing the expanded data to the address to determine when the address corresponds to an expanded datum of the expanded data; and

routing the address to a second memory array when the address and a datum from the decompressed data match.

5. A method as claimed in claim 4, further including a step of routing the address to the first memory array when the comparing step determines that the address does not match any datum from the decompressed or compressed data.

6. A method as claimed in claim 4, wherein the step of routing the address to a second memory array includes a step of reading data via the address.

7. A method as claimed in claim 4, wherein the step of routing the address to a second memory array includes a step of writing data via the address.

8. A method as claimed in claim 4 wherein the step of routing the address to a second memory array comprises a step of routing the address to a separate portion of the first memory array when the address and a datum from the decompressed data match.

9. A method for accessing a memory array, the method comprising steps of:

receiving a memory array access request including a requested address;

generating a first hash code from the requested address;

comparing the first hash code to hash codes for decompressed addresses stored in a temporary memory array;

determining if an address stored in the temporary array corresponds to the requested address when a match is found between a hash code for a decompressed address and the first hash code; and

routing the memory array access request to a spare memory array when an address stored in the temporary array corresponds to the requested address.

10. A method as claimed in claim 9, wherein, when the comparing step indicates that no match is found between the first hash code and the hash codes for decompressed addresses stored in the temporary memory array, the method includes steps of:

determining which portion of a map memory array to decompress, the map memory array storing compressed addresses of defective memory array cells in a first memory array;

decompressing compressed data from the portion to provide decompressed addresses; and

storing the decompressed address in the temporary memory array.

11. A method as claimed in claim 10, wherein the step of decompressing compressed data includes a step of generating a hash code for each decompressed address, and wherein the method further comprises a step of comparing the first hash code to the hash codes for the decompressed addresses stored in the temporary memory array.

12. A method as claimed in claim 11 wherein, when a match is found between a hash code for a decompressed address and the first hash code, the method includes a step of routing the memory array address request to the spare memory array.

13. A method as claimed in claim 12, further comprising a step of sending a wait command prior to said step of determining which portion of a map memory array to decompress.

14. A method as claimed in claim 13, further comprising a step of sending a cancel wait command prior to said step of routing the memory array address request to the spare memory array.

15. A method as claimed in claim 12 wherein, when no match is found between the first hash code and the hash codes for the decompressed addresses stored in the temporary memory array, the method includes steps of:

sending a cancel wait command; and

routing the memory array access request to the first memory array.

16. A method as claimed in claim 15 wherein:

the step of receiving a memory array access request includes a step of receiving a memory array access request including a requested address from a processor;

the step of sending a wait command includes a step of sending a wait command to the processor; and

the step of sending a cancel wait command includes a step of sending a cancel wait command to the processor.

17. A method for identifying defective cells in a memory array, the method comprising steps of:

receiving a request for accessing an address;

analyzing the address to determine when the address matches an address stored in a temporary memory array, and, when the address does not match any address stored in the temporary memory array, performing steps of:

analyzing the address to determine which portion of compressed data stored in a map memory array containing compressed addresses of defective cells in a first memory array to decompress;

decompressing the portion of compressed data to provide expanded data;

writing the expanded data to the temporary memory array; and

comparing the expanded data to the address to determine when the address corresponds to an expanded datum of the expanded data.

18. A method as claimed in claim 17, further comprising a step of routing the address to a first memory array when the address does not match any address stored in the temporary memory array or to an expanded datum of the expanded data.

19. A method as claimed in claim 17, further comprising a step of routing the address to a second memory array when the step of analyzing the address determines that the address matches an address stored in the temporary memory array.

20. A method as claimed in claim 17, further comprising a step of routing the address to a second memory array when the step of comparing the expanded data to the address determines that the address corresponds to an expanded datum of the expanded data or to an address stored in the temporary memory array.

21. A memory control circuit comprising:

storage control unit means coupled to a bus, the storage control unit means for accessing memory array units to retrieve data from a first memory array unit in response to memory array access requests delivered via the bus;

first memory array means coupled to the storage control unit means, the first memory array means for storing data;

second memory array means coupled to the storage control unit means, the second memory array means for replacing cells determined to be defective in the first memory array means; and

means for compressing data describing memory array addresses corresponding to cells determined to be defective in the first memory array means to provide compressed addresses and for decompressing compressed addresses to

provide decompressed addresses, the compressing means coupled to the storage control unit means.

22. A memory control circuit as claimed in claim 21, further comprising third memory array means for storing the compressed addresses, the third memory array means coupled to the compressing means.

23. A memory control circuit as claimed in claim 22, further comprising fourth memory array means coupled to the storage control unit means, the fourth memory array means for temporarily storing the decompressed addresses from the compressing means.

24. A memory control circuit as claimed in claim 23 wherein the first, second, third and fourth memory array means comprise random-access memories.

25. A memory control circuit as claimed in claim 23 wherein the compressing means is for:

identifying a starting and an ending address for a group of adjacent defective cell sites in the first memory array means;

reconfiguring the addresses of the group as the starting address and a difference between the starting address and the ending address to provide compressed addresses; and

supplying the compressed addresses to the third memory array means.

26. A memory control circuit as claimed in claim 25 wherein the compressing means is further for:

accepting addresses of a group of adjacent addresses describing defective cell sites in the first memory array means as a starting address and a difference between the starting address and the ending address; and

reconstructing individual addresses of the defective cell sites to provide decompressed addresses.

27. A memory control circuit as claimed in claim 25 wherein the compressing means is additionally for writing the decompressed addresses to the fourth memory array means.

28. A memory control circuit as claimed in claim 21 wherein the storage control unit means, the first memory array means, the second memory array means, the compressing means and the third memory array means comprise an integrated circuit.

29. A memory control circuit comprising:

a storage control unit coupled to a bus, the storage control unit for accessing memory array units to retrieve data from a first memory array unit in response to memory array access requests delivered via the bus;

a first memory array coupled to the storage control unit, the first memory array for storing data;

a second memory array coupled to the storage control unit, the second memory array for replacing cells determined to be defective in the first memory array; and

a data compressor that compresses data describing memory array addresses corresponding to cells determined to be defective in the first memory array to provide compressed addresses and that decompresses compressed addresses to provide decompressed addresses, the data compressor coupled to the storage control unit.

30. A memory control circuit as claimed in claim 29, further comprising a third memory array for storing the compressed addresses, the third memory array coupled to the data compressor.

31. A memory control circuit as claimed in claim 30, further comprising a fourth memory array coupled to the storage control unit, the fourth memory array for temporarily storing the decompressed addresses from the data compressor.

32. A memory control circuit as claimed in claim 31 wherein the first, second, third and fourth memory arrays comprise random-access memories.

33. A memory control circuit as claimed in claim 31 wherein the data compressor identifies a starting and an ending address for a group of adjacent defective cell sites in the first memory array, reconfigures the addresses of the group as the starting address and a difference between the starting address and the ending address to provide compressed addresses and supplies the compressed addresses to the third memory array.

34. A memory control circuit as claimed in claim 33 wherein the data compressor further accepts addresses of a group of adjacent addresses describing defective cell sites in the first memory array as a starting address and a difference between the starting address and the ending address and reconstructs individual addresses of the defective cell sites to provide decompressed addresses.

35. A memory control circuit as claimed in claim 33 wherein the compressing means is additionally for writing the decompressed addresses to the fourth memory array.

36. A memory control circuit as claimed in claim 28, wherein the storage control unit, the first memory array, the second memory array, the data compressor and the third memory array comprise an integrated circuit.

37. A computer comprising:

a processor;

a read-only memory storing instructions for operation of the processor;

a random-access memory array storing data;

a spare random-access memory array storing data corresponding to defective locations in the random-access memory array;

a storage control unit coupled to the processor, the read-only memory, the random-access memory and the spare random-access memory, the storage control unit accessing the read-only memory, the random-access memory and the spare random-access memory to retrieve data in response to commands from the processor; and

a data compressor coupled to the storage control unit, the data compressor compressing data indicative of addresses of defective storage locations in the random access memory array to provide compressed addresses, and decompressing the compressed addresses.

38. A computer as claimed in claim 37 wherein the data compressor comprises the processor executing instructions stored in the read-only memory.

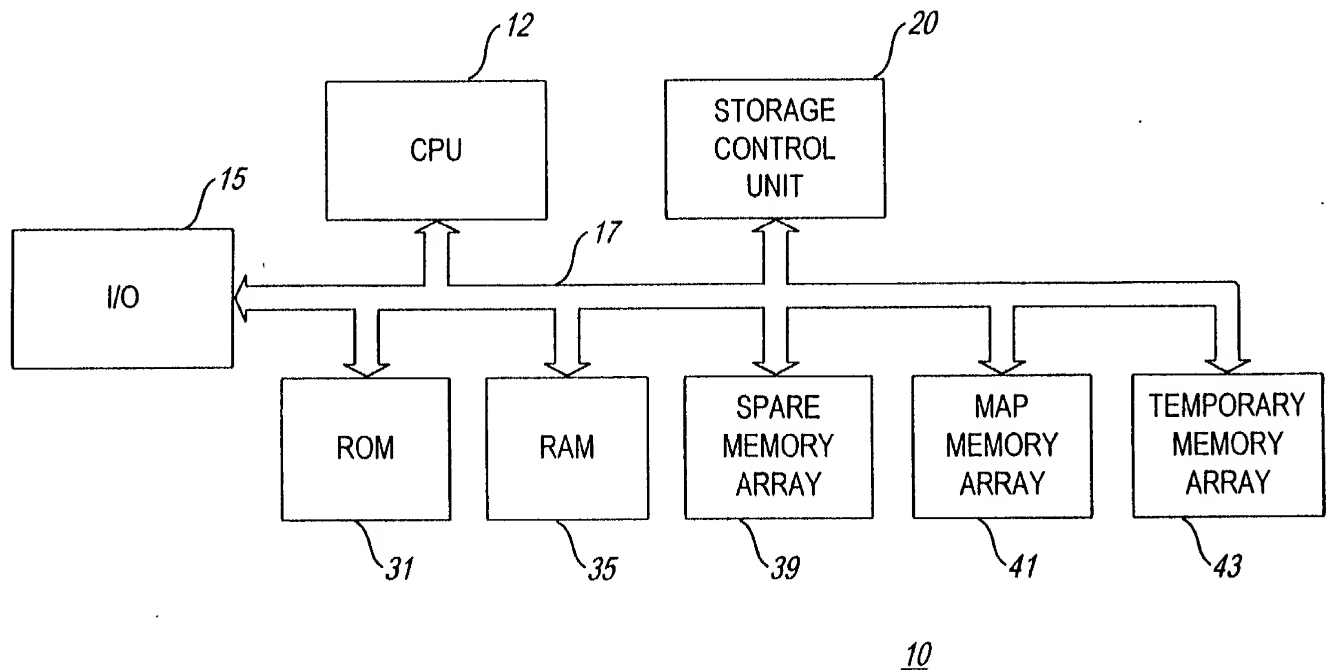
39. A computer as claimed in claim 37 wherein the data compressor comprises circuitry incorporated within the storage control unit.

40. A computer as claimed in claim 37 wherein the data compressor comprises circuitry incorporated within the random-access memory array.

METHOD AND APPARATUS FOR REDUNDANT LOCATION ADDRESSING USING DATA COMPRESSION

ABSTRACT OF THE DISCLOSURE

A method and apparatus for identifying defective cells in a memory array includes receiving a request for accessing an address and analyzing the address to determine when the address matches an address stored in a temporary memory array. When the address does not match any address stored in the temporary memory array, a wait instruction is sent to a processor and the address is analyzed to determine which portion of compressed data stored in a map memory array to decompress. The map memory array stores data containing compressed addresses of defective cells in a first memory array. The portion of compressed data is then decompressed to provide expanded data when the address does not match any address stored in the temporary memory array. The expanded data are then written to the temporary memory array, and the expanded data are compared to the address to determine when the address corresponds to an expanded datum of the expanded data.



CPU
12
STORAGE CONTROL UNIT
20
I/O
15
17
ROM
31
RAM
35
SPARE MEMORY ARRAY
39
MAP MEMORY ARRAY
41
TEMPORARY MEMORY ARRAY
43
10

Fig. 1

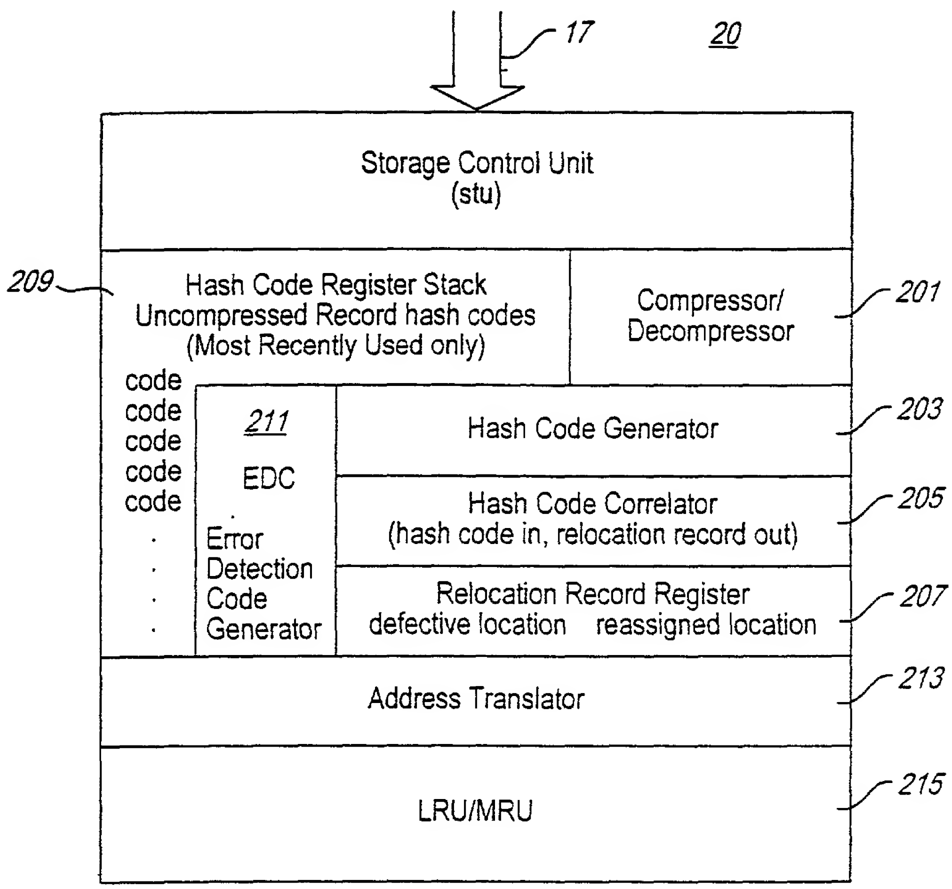

17
20
Storage Control Unit
(stu)
209
Hash Code Register Stack
Uncompressed Record hash codes
(Most Recently Used only)
Compressor/
Decompressor
201
code
code
code
code
code
211
EDC
Error
Detection
Code
Generator
Hash Code Generator
203
Hash Code Correlator
(hash code in, relocation record out)
205
Relocation Record Register
defective location reassigned location
207
Address Translator
213
LRU/MRU
215

Fig. 2

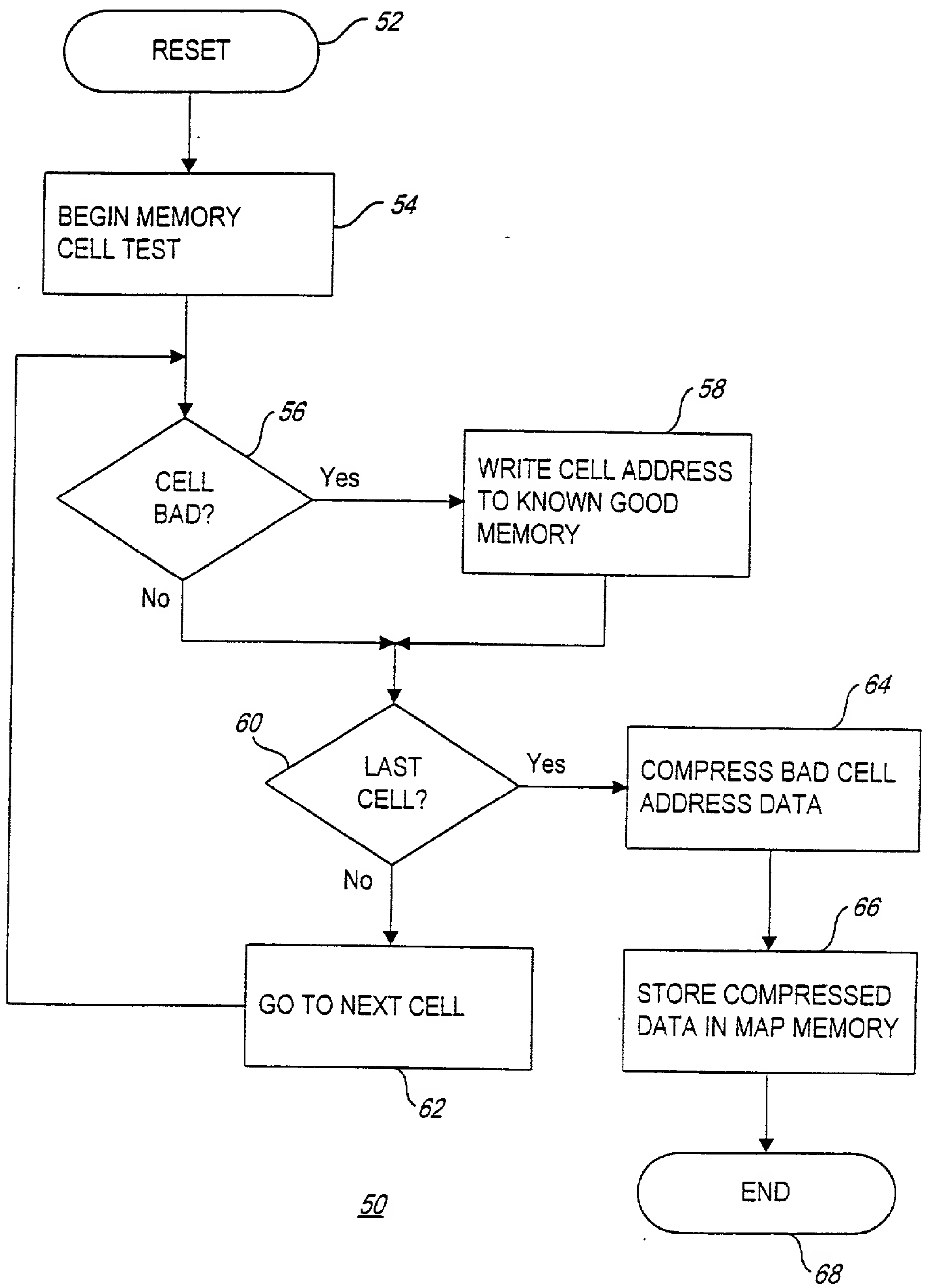

RESET
52
BEGIN MEMORY CELL TEST
54
CELL BAD?
56
Yes
No
WRITE CELL ADDRESS TO KNOWN GOOD MEMORY
58
LAST CELL?
60
Yes
No
COMPRESS BAD CELL ADDRESS DATA
64
GO TO NEXT CELL
62
STORE COMPRESSED DATA IN MAP MEMORY
66
END
68
50

Fig. 3

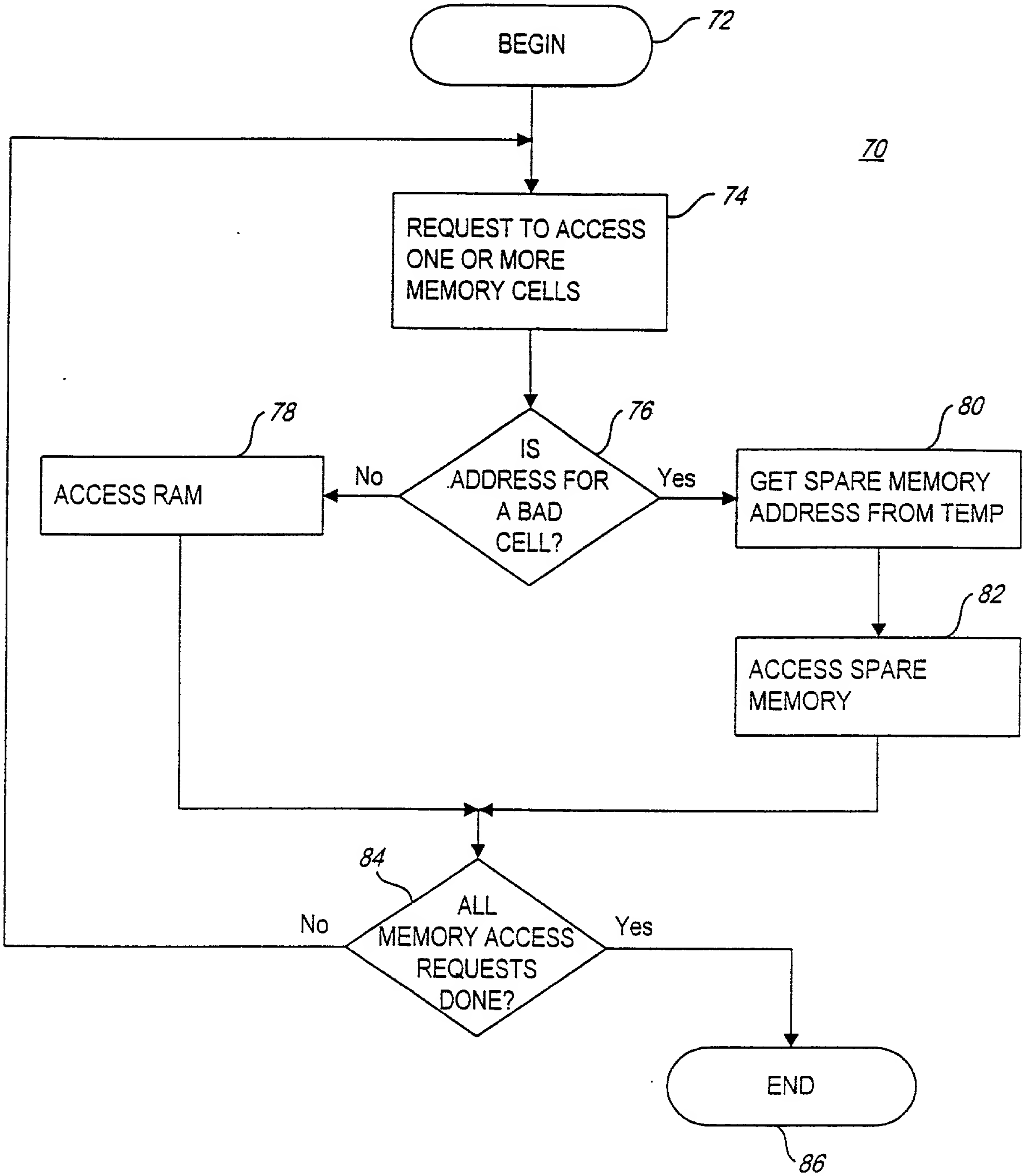

BEGIN
72
70
REQUEST TO ACCESS ONE OR MORE MEMORY CELLS
74
IS ADDRESS FOR A BAD CELL?
76
No
Yes
ACCESS RAM
78
GET SPARE MEMORY ADDRESS FROM TEMP
80
ACCESS SPARE MEMORY
82
ALL MEMORY ACCESS REQUESTS DONE?
84
No
Yes
END
86

Fig. 4

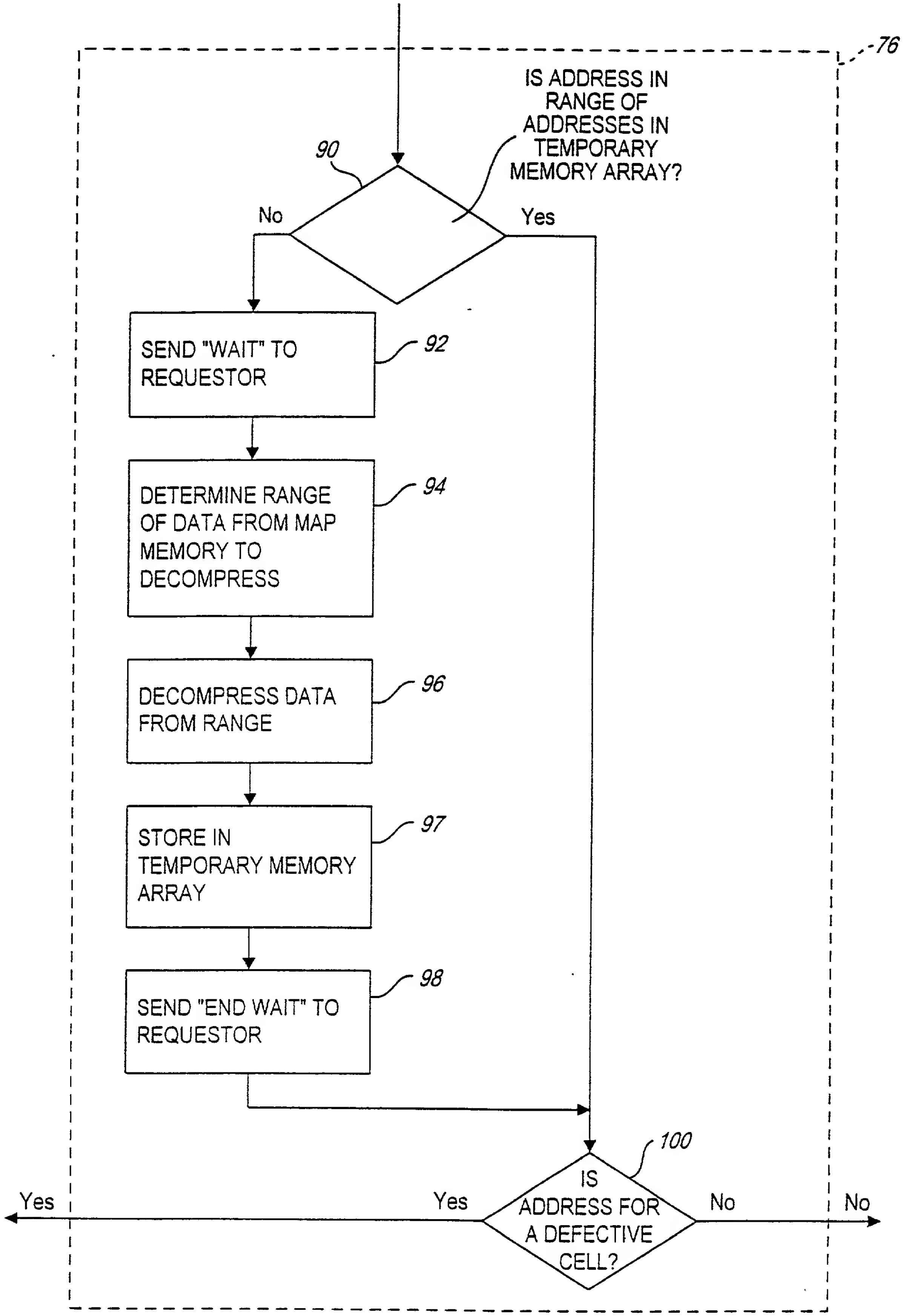

76
IS ADDRESS IN RANGE OF ADDRESSES IN TEMPORARY MEMORY ARRAY?
90
No
Yes
SEND "WAIT" TO REQUESTOR
92
DETERMINE RANGE OF DATA FROM MAP MEMORY TO DECOMPRESS
94
DECOMPRESS DATA FROM RANGE
96
STORE IN TEMPORARY MEMORY ARRAY
97
SEND "END WAIT" TO REQUESTOR
98
100
IS ADDRESS FOR A DEFECTIVE CELL?
Yes
Yes
No
No

Fig. 5

Express Mail No. EL673947162US

DECLARATION

As the below-named inventor, I declare that:

My residence, post office address, and citizenship are as stated below under my name.

I believe I am the original, first, and sole inventor of the invention entitled "METHOD AND APPARATUS FOR REDUNDANT LOCATION ADDRESSING USING DATA COMPRESSION," which is described and claimed in the foregoing specification and for which a patent is sought.

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to herein (if any).

I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application in accordance with 37 C.F.R. § 1.56(a).

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

Thomas W. Voshell

THOMAS W. VOSHELL

Date 1-9-98

Residence	:	City of Boise, County of Ada State of Idaho
Citizenship	:	United States of America
P.O. Address	:	1227 E. Woodvine Court Boise, Idaho 83706

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(660073.549)

Express Mail No. EL673947162US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Thomas W. Voshell
Filed	:	
For	:	METHOD AND APPARATUS FOR REDUNDANT LOCATION ADDRESSING USING DATA COMPRESSION

Docket No.	:	660073.549
Date	:	

Box Patent Application
Assistant Commissioner for Patents
2011 Jefferson Davis Highway
Washington, DC 20231

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment filed concurrently herewith, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventors.

Assignee hereby appoints RICHARD W. SEED, Registration No. 16,557; ROBERT J. BAYNHAM, Registration No. 22,846; EDWARD W. BULCHIS, Registration No. 26,847; GEORGE C. RONDEAU, JR., Registration No. 28,893; DAVID H. DEITS, Registration No. 28,066; WILLIAM O. FERRON, JR., Registration No. 30,633; PAUL T. MEIKLEJOHN, Registration No. 26,569; DAVID J. MAKI, Registration No. 31,392; RICHARD G. SHARKEY, Registration No. 32,629; DAVID V. CARLSON, Registration No. 31,153; MAURICE J. PIRIO, Registration No. 33,273; KARL R. HERMANNS, Registration No. 33,507; DAVID D. McMASTERS, Registration No. 33,963; ROBERT IANNUCCI, Registration No. 33,514; JOSHUA KING, Registration No. 35,570; MICHAEL J. DONOHUE, Registration No. 35,859; CHRISTOPHER J. DALEY-WATSON,

Registration No. 34,807; STEVEN D. LAWRENZ, Registration No. 37,376; ROBERT G. WOOLSTON, Registration No. 37,263; ELLEN M. BIERMAN, Registration No. 38,079; BRYAN A. SANTARELLI, Registration No. 37,560; CAROL NOTTENBURG, Registration No. 39,317; CRAIG S. JEPSON, Registration No. 33,517; PAUL T. PARKER, Registration No. 38,264; JOHN C. STEWART, Registration No. 40,188; ROBERT W. BERGSTROM, Registration No. 39,906; DAVID W. PARKER, Registration No. 37,414; ROBERT E. MATES, Registration No. 35,271; BRIAN G. BODINE, Registration No. 40,520; FRANK ABRAMONTE, Registration No. 38,066; E. RUSSELL TARLETON, Registration No. 31,800; FREDERICK M. FLIEGEL, Registration No. 36,138; JAN C. L. MAXWELL, Registration No. 41,181; THOMAS L. EWING, Registration No. 34,328; CLIFTON G. GREEN, Registration No. 41,044; and PHILLIP B. C. JONES, Registration No. 38,195, comprising the firm of SEED AND BERRY LLP, 6300 Columbia Center, Seattle, Washington 98104-7092; along with MICHAEL L. LYNCH, Registration No. 30,871; LIA M. PAPPAS, Registration No. 34,095; W. ERIC WEBOSTAD, Registration No. 35,406; WALTER D. FIELDS, Registration No. 37,130; CHARLES B. BRANTLEY, II, Registration No. 38,086; SUSAN B. COLLIER, Registration No. 34,566, KEVIN D. MARTIN, Registration No. 37,882; and DAVID J. PAUL, Registration No. 34,692, of Micron Technology, Inc., 8000 South Federal Way, Boise, Idaho 83706-9632, as its attorneys to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. Please direct all telephone calls to Bryan A. Santarelli at (206) 622-4900 and telecopies to (206) 682-6031.

Please direct all communications to:

Frederick M. Fliegel, Esq.
Seed and Berry LLP
6300 Columbia Tower
701 Fifth Avenue
Seattle, Washington 98104-7092

Pursuant to 37 C.F.R. § 3.73, the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the

Assignment to MICRON TECHNOLOGY, INC., filed concurrently herewith for recording, a copy of which is attached hereto, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

MICRON TECHNOLOGY, INC.
ASSIGNEE

Jan 19, 1998
DATE

Enclosure:
Copy of Assignment

c:\FMF\97-0071

Express Mail No. EL673947162US
PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, DC 20231.

March 6, 2000
Date

Michele Coleman-Owens
Michele Coleman-Owens

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Thomas W. Voshell	Attorney Docket No.	: 500080.01 (660073.549)
Serial No.	: 09/012,036	Group Art Unit	: 2784
Filed	: January 22, 1998	Examiner	: S. Lin
Title	: METHOD AND APPARATUS FOR REDUNDANT LOCATION ADDRESSING USING DATA COMPRESSION		

TRANSMITTAL FOR REVOCATION AND SUBSTITUTE POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith and attached hereto as Addendum A is a true and correct copy of the Revocation and Substitute Power of Attorney executed January 3, 2000, in the above-identified application. The above-identified application is identified on Exhibit A.

Pursuant to 37 C.F.R. § 3.73, Michael L. Lynch, duly authorized designee of Assignee, has certified that the evidentiary documents have been reviewed, specifically the Assignment to MICRON TECHNOLOGY, INC., recorded January 22, 1998 , under Reel 8974 / Frame 0193, and certified that to the best of his knowledge and belief, title remains in the name of the Assignee.

Respectfully submitted,

DORSEY & WHITNEY LLP

Kimton N. Eng
Kimton N. Eng
Registration No. 43,605

KNE:mco

Enclosures:
Addendum A
Exhibit A

1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101-4010
(206) 903-8800 (telephone)
(206) 903-8200 (fax)

PATENT

ADDENDUM A

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Assistant Commissioner for Patents
Washington, DC 20231

REVOCATION AND SUBSTITUTE POWER OF ATTORNEY

Sir:

In the matter of the patent applications identified in Exhibit A attached hereto, I, MICHAEL L. LYNCH, declare that I am a duly authorized designee of Micron Technology, Inc., the ASSIGNEE of the entire right, title and interest in and to the above-referenced patent applications. Documentary evidence of chain of title from the original owner to ASSIGNEE has been or is concurrently being filed with and recorded by the United States Patent Office. The evidentiary documents referred to in the instant Revocation and Power of Attorney have been reviewed by the undersigned, and it is certified that, to the best of ASSIGNEE's knowledge and belief, title is held solely in and by ASSIGNEE.

On behalf ASSIGNEE, I revoke all power of attorney heretofore given, and hereby appoint EDWARD W. BULCHIS, Reg. No. 26,847; JON F. TUTTLE, Reg. No. 25,713; PAUL T. MEIKLEJOHN, Reg. No. 26,569; GLENN P. RICKARDS, Reg. No. 29,428; DALE C. BARR, Reg. No. 40,498; KIMTON N. ENG, Reg. No. 43,605; DAVID E. BOONE, Reg. No. 27,857; SCOTT W. DOYLE, Reg. No. 39,176; REED R. HEIMBECHER, Reg. No. 36,353; JOHN T. KENNEDY, Reg. No. 42,717; GREGORY D. LEIBOLD, Reg. No. 36,408; GARY M. POLUMBUS, Reg. No. 25,364; THOMAS H. YOUNG, Reg. No. 25,796; W. ROBINSON H. CLARK, Reg. No. 41,530; GREGORY J. GLOVER, Reg. No. 34,173; JOHN K. HARROP, Reg. No. 41,817; CHRIS McWHINNEY, Reg. No. 42,875; ALDO NOTO, Reg. No. 35,628; MATTHEW PHILLIPS, Reg. No. 43,403; JOHN W. RYAN, Reg. No. 33,771; AMI P. SHAH,

Reg. No. 42,143; SEAN S. WOODEN, Reg. No. 43,997; MICI EL C. GILCHRIST, Reg. No. 40,619; BRIAN J. LAURENZO, Reg. No. 34,207; SHANE COLEMAN, Reg. No. 44,623; RONALD J. BROWN, Reg. No. 29,016; DAVID E. BRUHN, Reg. No. 36,762; DAVID N. FRONEK, Reg. No. 25,678; JOSEPH F. HAAG, Reg. No. 42,612; STUART R. HEMPHILL, Reg. No. 28,084; GRANT A. JOHNSON, Reg. No. 42,696; KENNETH E. LEVITT, Reg. No. 39,747; NIALL A. MACLEOD, Reg. No. 41,963; SCOTT A. MARKS, Reg. No. 44,902; DEVAN V. PADMANABHAN, Reg. No. 38,262; GERALD H. SULLIVAN, Reg. No. 36,311; BRIAN PARK, Reg. No. P-45,519; MARK W. ROBERTS, Reg. No. P-46,160; STEVEN H. ARTERBERRY, Reg. No. P-46,314; of the firm of DORSEY & WHITNEY LLP; along with MICHAEL L. LYNCH, Reg. No. 30,871; LIA M. PAPPAS, Reg. No. 34,095; WALTER D. FIELDS, Reg. No. 37,130; CHARLES B. BRANTLEY, II, Reg. No. 38,086; KEVIN D. MARTIN, Reg. No. 37,882; and DAVID J. PAUL, Reg. No. 34,692, of MICRON TECHNOLOGY, INC., 8000 South Federal Way, Boise, Idaho 83706-9632, as its attorneys to transact all business in the Patent and Trademark Office connected therewith.

Please direct all future correspondence and telephone calls to:

Edward W. Bulchis
DORSEY and WHITNEY LLP
U.S. Bank Centre, Suite 3400
1420 Fifth Avenue
Seattle, Washington 98101
(206)903-8800
(206)903-8820 facsimile.

ASSIGNEE:

Micron Technology, Inc.

Jan 3, 2000
Date

By
Michael L. Lynch
Chief Patent Counsel

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EXHIBIT A

09/012,036	660073.549	Thomas W. Voshell	22-Jan-98	Data Compression for Redundant Location Addressing